	Document ID	Issue Date	Pages	Title	Current OR
1	US 20040103218 A1	20040527	52	Novel massively parallel supercomputer	709/249
2	US 20040012600 A1	20040122	72	Scalable high performance 3d graphics	345/506
3	US 20030221179 A1	20031127	13	System and method for placing clock drivers in a standard cell block	716/18
4	US 20030212975 A1	20031113	14	System and methods for placing clock buffers in a datapath stack	716/10
5	US 20030163750 A1	20030828	17	Clock grid skew reduction technique using biasable delay drivers	713/503
6	US 20030131334 A1	20030710	37	Synthesis strategies based on the appropriate use of inductance effects	716/12
7	US 20030110462 A1	20030612	11	Method for reducing design effect of wearout mechanisms on signal skew in integrated circuit design	716/6
8	US 20030101307 A1	20030529	183	System of distributed microprocessor interfaces toward macro-cell based designs implemented as ASIC or FPGA bread boarding and relative common bus protocol	710/305
9	US 20030074643 A1	20030417	14	Unified database system to store, combine, and manipulate clock related data for grid-based clock distribution design	716/6
10	US 20030074642 A1	20030417	17	Clock skew verification methodology for grid-based design	716/6
11	US 20030074175 A1	20030417	16	Simulation by parts method for grid-based clock distribution design	703/19
12	US 20020087940 A1	20020704	32	Method for designing large standard-cell based integrated circuits	716/2

	Document ID	Issue Date	Pages	Title	Current OR
13	US 20020087939 A1	20020704	32	Method for designing large standard-cell based integrated circuits	716/2
14	US 20010010090 A1	20010726	22	Method for design optimization using logical and physical information	716/2
15	US 6732343 B2	20040504	14	System and methods for placing clock buffers in a datapath stack	716/10
16	US 6651230 B2	20031118	12	Method for reducing design effect of wearout mechanisms on signal skew in integrated circuit design	716/6
17	US 6591402 B1	20030708	60	System and method for performing assertion-based analysis of circuit designs	716/5
18	US 6567967 B2	20030520	32	Method for designing large standard-cell base integrated circuits	716/10
19	US 6557145 B2	20030429	20	Method for design optimization using logical and physical information	716/2
20	US 6320436 B1	20011120	12	Clock skew removal apparatus	327/158
21	US 6311313 B1	20011030	22	X-Y grid tree clock distribution network with tunable tree and grid networks	716/6
22	US 6205571 B1	20010320	20	X-Y grid tree tuning method	716/2
23	US 6144224 A	20001107	18	Clock distribution network with dual wire routing	326/93
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	Document ID	Issue Date	Pages	Title	Current OR
26	US 5878055 A	19990302	14	Method and apparatus for verifying a single phase clocking system including testing for latch early mode	714/744
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31	US 4242730 A	19801230	86	Single scan microprocessor-controlled densitometer	356/39
32	US 3785510 A	19740115	33	METHOD FOR THE DESTINATION CONTROL OF OBJECTS FED INTO A DISTRIBUTING CONVEYING SYSTEM AND DISTRIBUTING CONVEYING SYSTEM FOR PERFORMING SUCH METHOD	198/349.9
33	US 3641324 A	19720208	7	POSITION BUSY SIGNALING APPARATUS	700/78